IPSY200-XX-47 SERIES

APPLICATION NOTE VP AN15

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ABBREVIATIONS USED IN THIS APPLICATION NOTE

A/D	Analogue to Digital Converter
ATCA	Advanced Telecommunications Computing Architecture
CSA	Canadian Standards Association
EMI	Electromagentic Interference
FRU	Field Replaceable Units
IPCM	Input Power Conditioning Module
IPMC	Intelligent Platform Manager Controller
IPSY	Input Power System
MTBF	Mean Time Between Failure
PCIMG	PCI Industrial Computing Manufacturers Group
POLs	Point of load converters
SELV	Safety Extra Low Voltage
UL	Underwriters Laboratories
VBUS	Intermediate Voltage Bus

1. GENERAL INTRODUCTION

The IPSY200-XX-47 module is designed as a fully compliant input conditioning module for the dual redundant –48VDC feeds to an ATCA Front Board/Blade as per the PICMG 3.0 Specifications. The IPSY200-XX-47 series is also designed to produce a 3V3 supply for the IPMC and a 5V supply for the front panel blue LED with a combined power output of 6.6W. This is limited to 6.6W to ensure that the total input management power is below 10W before negotiations begin for turning on the VBUS output.

The voltage of the VBUS output in this module is stated by numerical value of the XX fields in the part number. The most common value of the VBUS in ATCA applications is 12V and for the rest of this application note the value of VBUS will be referred to as 12V. Using the fact that each card in an ATCA system is limited to 200W input power this means that the 12V VBUS output has a range of 0-15A. The VBUS output can then be fed to either dc-dc converters or POLs to gain a quick and simple solution to whatever power supply requirements are required in the computer architecture.

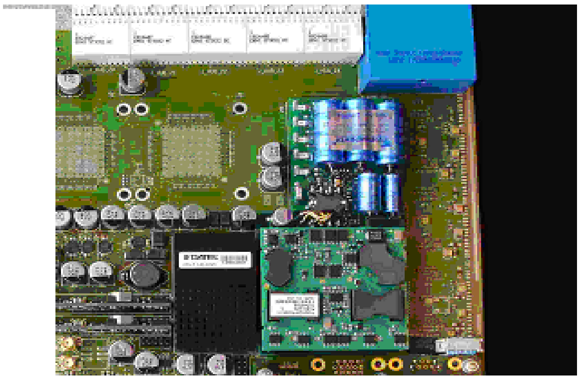
The PICMG 3.0 specification has been identified to define open architecture modular computing components that can be quickly integrated to deploy high performance services solutions. This has been achieved by providing detailed information on mechanicals, systems management, power distribution, Data I/O, thermal and regulatory requirements. The IPSY200-XX-47 module has been designed so that the 48V primary side voltages are restricted to within the zone 1 area of the ATCA blade thereby avoiding clearance and creepage problems associated with the input circuitry.

2. MECHANICAL

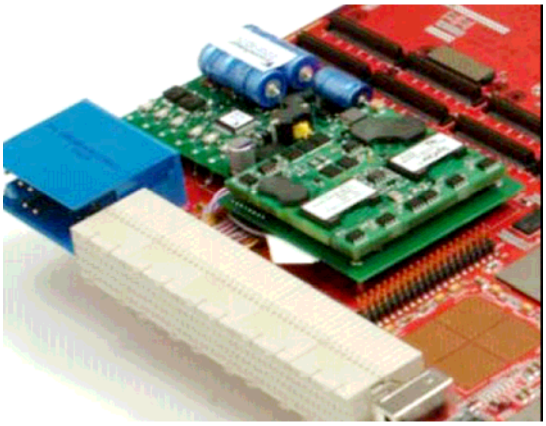
2.1. MECHANICAL DESIGN

The IPSY200-XX-47 assembly consists of a single mezzanine card containing the VISIONPOWER IPCM module and a SYNQOR PQ60120HPA20NK7 module. The overall height of the IPSY200-XX-12 module is 19.5mm this meets the component side 1 height requirements of PICMG 3.0 of 21.35mm. The fact that this height is 1.85mm less than the PICMG 3.0 requirements means that if required a cover could be fitted on to the ATCA blade.

The reason behind the unique L shape of the IPSY200-XX-12 module is to ensure that the 48V primary side voltages are restricted to within the zone 1 area of the ATCA front board. Connectivity to the ATCA blade is via a combination of solder pins and a Samtec 2mm pitch header. The exact location of the connections can be seen in section 2.2 of application note.



Perpendicular to Zone 1 connector



Parallel to zone 1 connector

Figure 1: Typical ATCA applications

2.2. MECHANICAL OUTLINE

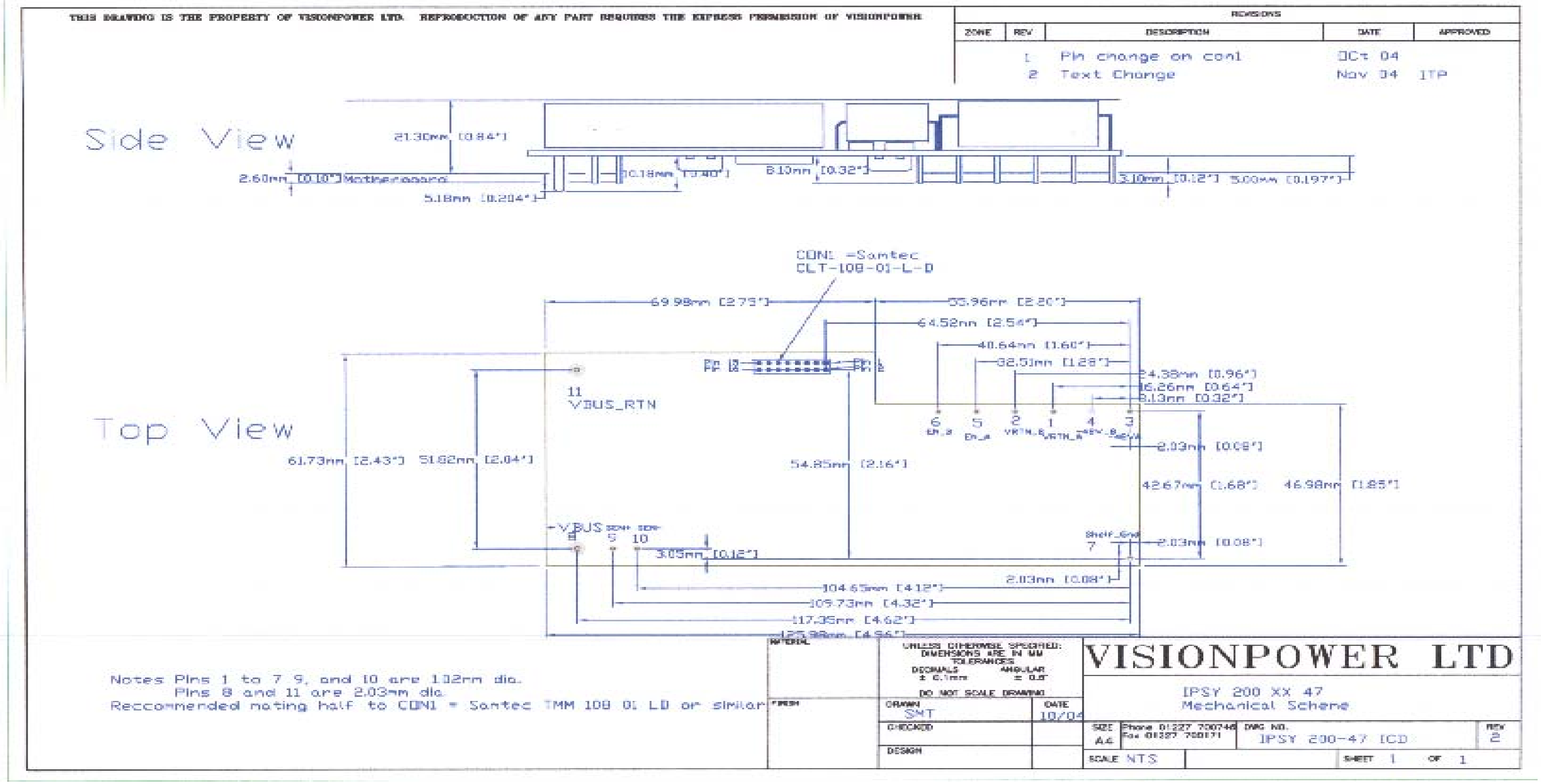


Figure 2: Layout and side view of IPSY200-12-47

2.3. MODEL NUMBER CONVENTIONS

The breakdown of the part number for the IPSY series is as follows:

IPSY	PPP	XXX	WW	A
Series	Input Power i.e. 120 is 120W, 200 is 200W	VBUS rating of VBUS i.e. 3.3 is 3.3V, 12 is 12V	Width of module at zone 1 area: Blank means 55mm standard module.	Other Options

2.4. MODELS IN SERIES

There are currently 10 units available in the IPSY range. The main difference between the different models is a standard third party half brick module of the appropriate output voltage.

MODEL NO:	INPUT POWER	VBUS	WIDTH
IPSY200-12	200	12	55
IPSY200-5	200	5.0	55
IPSY200-3V3	200	3.3	55
IPSY200-2V5	200	2.5	55
IPSY200-1V8	200	1.8	55
IPSY200-12-47	200	12	47
IPSY200-5-47	200	5.0	47
IPSY200-3V3-47	200	3.3	47
IPSY200-2V5-47	200	2.5	47
IPSY200-1V8-47	200	1.8	47

Table 1: Models in series

3. SAFETY CONSIDERATIONS

3.1. INTRODUCTION

For the ATCA Front Board to gain safety agency approval the IPSY200-XX-12 must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL 60950-1, CSA C22.2 No. 60950-1-03 and VDE0850:2001-12(EN60950-1)

3.2. FUSING

The IPSY200-XX-47 module meets all of the necessary safety agency requirements with regards to fusing. There are 6 very fast-acting fuses located on the IPSY200-XX-47 module. They all are located on the top side of the module and their exact locations are shown in figure 3.
Table 2 describes in full detail the fuses manufacturer and part number information as per the location drawing in figure 3.

Circuit Reference	Input connection	Manufacturer	Series	Part Number	Rating
F1	VRTNA	LITTELFUSE	NANO-FUSE	R451 010	125Vdc, 10A
F2	VRTNB	LITTELFUSE	NANO-FUSE	R451 010	125Vdc, 10A
F3	-48VA	LITTLEFUSE	NANO-FUSE	R451 008	125Vdc, 8A
F4	-48VB	LITTELFUSE	NANO-FUSE	R451 008	125Vdc, 8A
F5	ENABLE A	LITTELFUSE	NANO-FUSE	R451.375	125Vdc, 375mA
F6	ENABLE B	LITTELFUSE	NANO-FUSE	R451.375	125Vdc, 375mA

Table 2: IPSY200-XX-12 fusing information

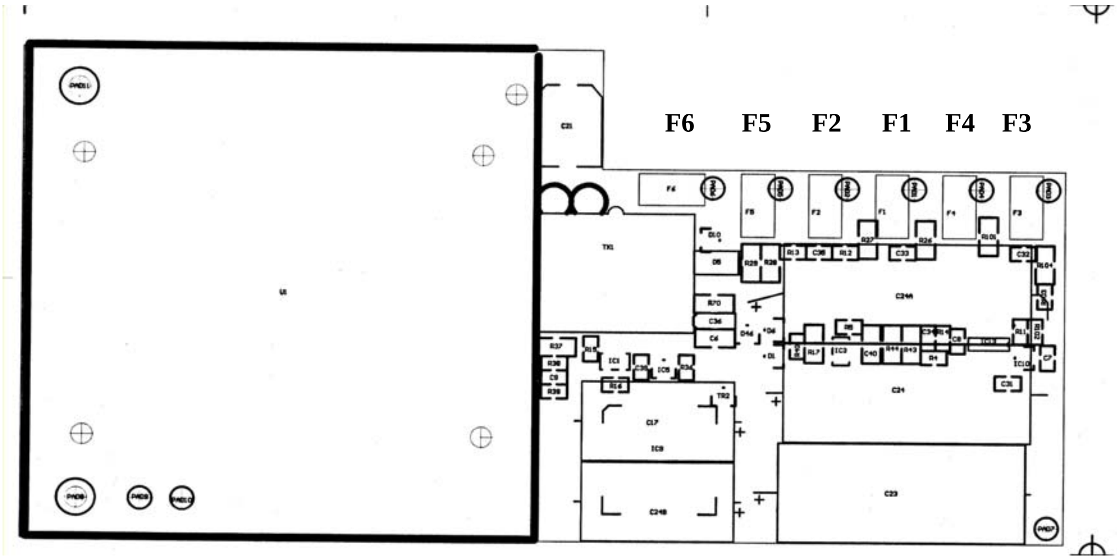


Figure 3: IPSY200-XX-47 fusing location drawing

3.3. EMC

The IPSY200-XX-47 module contains an EMI filter that is designed to meet the conducted emissions requirements of CISPR 22 Class B without the addition of any external components

3.4. SELV RATING

The IPSY200-XX-47 has been designed so that the Boost supply is always within SELV limits. This means that no hazardous voltages are present on the unit which need discharged to protect the user on turn off of the module.

4. ELECTRICAL PERFORMANCE

4.1. BASIC OPERATION OF POWER SUPPLY

The IPSY200-XX-47 module has been designed to be incorporated within an ATCA board to accept up to a maximum of 200W of input power via dual, redundant –48Vdc feeds from the zone 1 connector described in PICMG 3.0. Figure 4 shows a block diagram of the IPSY200-XX47 unit in an ATCA environment.

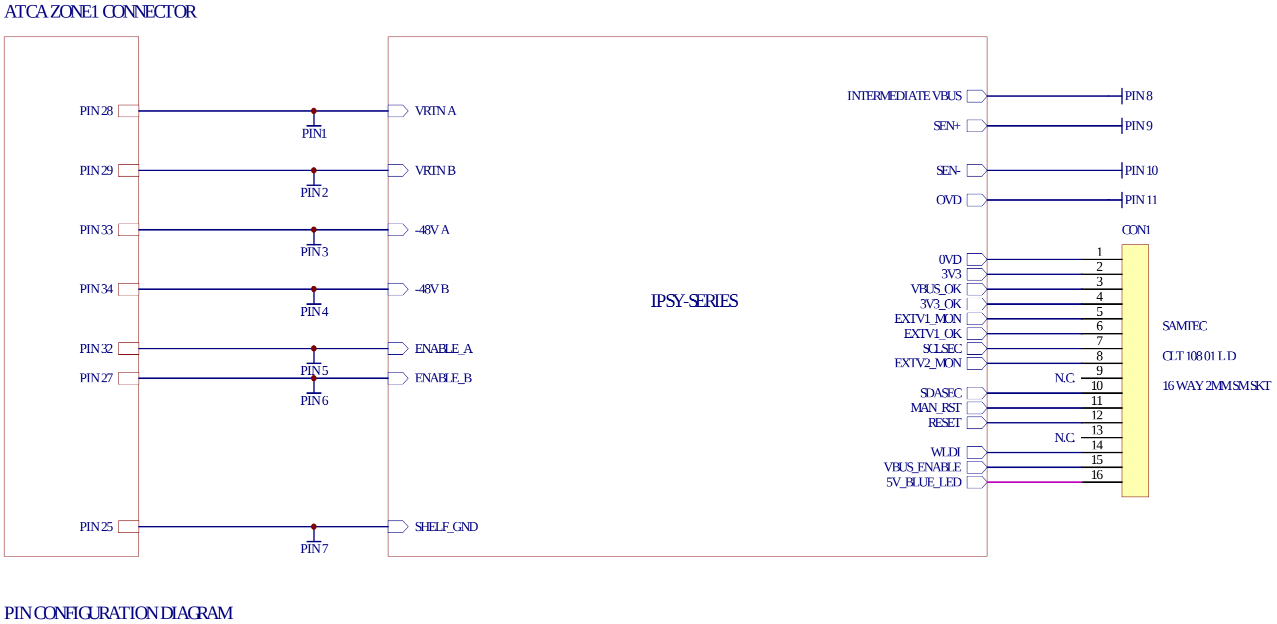


Figure 4: IPSY200-XX-47 IN ATCA APPLICATIONS

The following connections should be made from the zone 1 POSITRONIC connector to the IPSY200-XX-47 module in an ATCA application:

From zone 1 connector		Mating sequence on insertion	**IPSY200-XX-47 module**	
Pin #	Pin Designation		Pin #	Pin Designation
25	SHELF GND	FIRST	7	SHELF GND
27	ENABLE_B	FOURTH	6	ENABLE B
28	VRTN_A	FIRST	1	VRTN A
29	VRTN_B	FIRST	2	VRTN B
32	ENABLE_A	FOURTH	5	ENABLE A
33	-48V_A	SECOND	3	-48VA
34	-48V_B	THIRD	4	-48VB

Table 3: IPSY200-XX-12 Input Connections in ATCA applications

Due to the different lengths of the pins on the zone connector there is a defined power up sequence of ATCA boards that is as follows. The first pins to mate in the power connector are the ground pins and the VRTNA and VRTNB pins. The –48V_A and –48V_B inputs are then staggered so the power planes are not disturbed at the same time. The last pins to engage in the power sequence are the ENABLE pins. The ATCA backplane shall connect ENABLE_A to VRTN_A and ENABLE_B to VRTN_B.

After either of the ENABLE pins has connected to the backplane the IPSY200-XX-47 unit will provide a 3V3IPMC and a 5V blue LED output. The hold up bank of capacitors will start to charge up to 59.5V to meet the hold up requirements and the A/D converter and the output sequencing IC's will start to operate. The maximum total input power required for all these tasks is limited to 10W. The output connections of the IPSY200-XX-47 are shown in table 4. Keeping the VBUS_ENABLE to a logic HIGH level (referenced to 3V3) will keep the VBUS output disabled. A logic low signal will enable the VBUS output.

PIN NO	NAME	DESCRIPTION
1	VRTN A	-48VA input return orred in module with –48VB input return
2	VRTN B	-48V B input return orred in module with -48VA input return
3	-48VA	-48VA input orred in module with –48VB input
4	-48VB	-48VB input orred in module with –48VA input
5	ENABLE A	Connect to –48VA input return on shelf to enable module orred in module with Enable B
6	ENABLE B	Connect to –48VB input return on shelf to enable module orred in module with Enable A
7	SHELF GND	Connect to chassis connections on FRB to ensure proper earthing.
8	VBUS	Output power for Intermediate Bus
9	SEN+	Connect to 12V at load.
10	SEN-	Connect to 0VD at (12V) load return.
11	0VD	0V(12) RETURN power for intermediate Bus.
CON 1 1	0VD	0V (3V3) should be connected to 0V(VBUS)
CON 1 2	3V3	3V3 supply to power Intelligent Platform Manager
CON 1 3	VBUS OK	ACTIVE LOW indicates VBUS is in spec.
CON 1 4	3V3 OK	ACTIVE LOW indicates 3V3 is in spec.
CON 1 5	EXTV1_MON	Monitor point for external core rail 1.
CON 1 6	EXTV1_OK	ACTIVE LOW indicates external core rail 1 is in spec (Customer programmable)
CON 1 7	SCLSEC	Secondary side referenced I²C clock input. (referenced to 3V3 supply)
CON 1 8	EXTV2_MON	Monitor point for external core rail 2.
CON 1 9	N.C	No connection
CON 1 10	SDASEC	Secondary side referenced I²C data input/output for programming external core rail 1 and 2 monitoring. Also reading A to D outputs derived from – input 48VA,B,EnableA, ,B, –48V Input current and module temperature (referenced to 3V3 supply).
CON 1 11	MAN_RST	Low whenever RESET is low or when driven low. Stays low for programmable time in the range 25 to 200ms.
CON 1 12	RESET	ACTIVE LOW open drain output which is low whenever an enabled under or overvoltage condition exists on 3V3, 12V, EXTV1, or EXTV2.
CON 1 13	N.C	No connection
CON 1 14	WLD1	Watchdog timer input. High to Low transition clears the watchdog timer. Programmable from "OFF" to 6.4 seconds.
CON 1 15	VBUS _ENABLE	Module enable input. Logic low (referenced to (3V3) enables 12V converter.
CON 1 16	5V_BLUE_LED	5V supply for Blue LED

Table 4: IPSY200-XX-12 Output Connections in ATCA applications

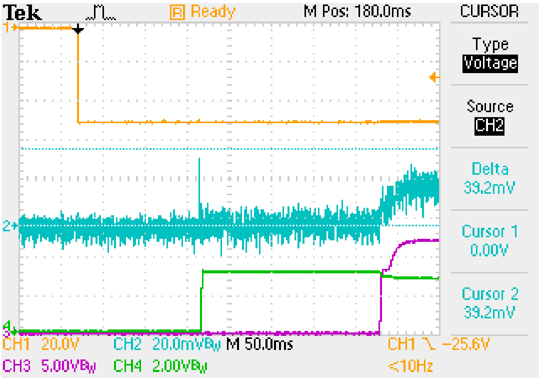
A logic low signal applied to pin 15 of connector 1 after mating has been completed will make a total of 200W of input power available for ATCA applications.

4.2. INRUSH CURRENT

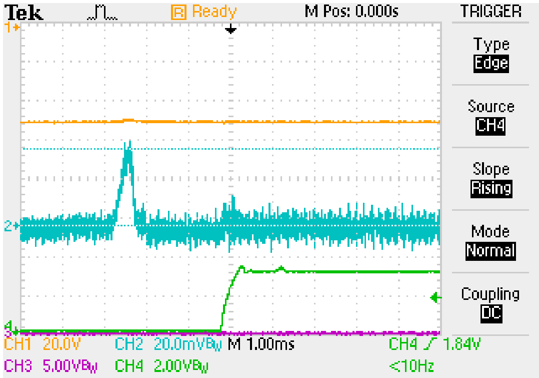
The IPSY200-XX-12 has been designed to limit the inrush current on turn on to within x5 of the nominal operating current. In this instance that is 20A. Due to the unique design of this module only 68µF of capacitance is placed directly across the input supply compared to the several thousand µF of capacitance which would normally be fitted to meet the 8.4ms of hold up.

A reservoir bank, isolated from the input, of 1560µF is slowly charged to a regulated supply of 59.5V by a 6k8 resistor in this module which means that on turn the amount of energy required to initial charge input capacitance has reduced greatly.

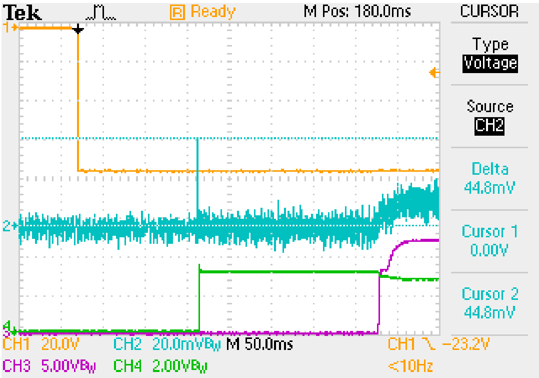
The 4 plots below shows the inrush current demanded on the unit with an input voltage of 48V and 72V. The current waveforms on ch2 are scaled at 2A/10mV and the peak currents can be calculated accordingly.

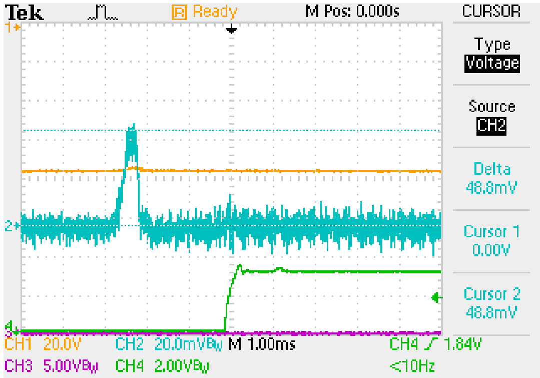


Plot 1: 48V input



Plot 2: 48V input





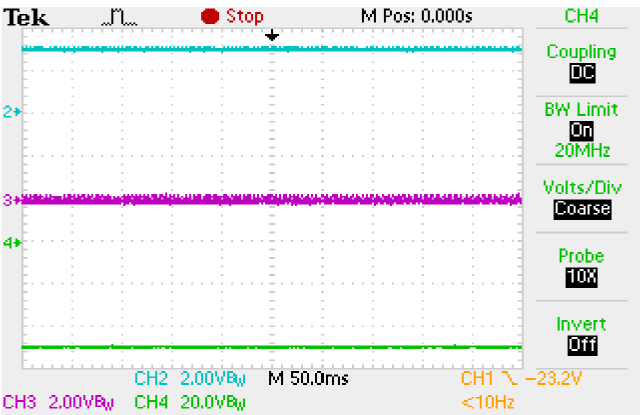
Plot 3: 72V input

Plot 4: 72V input

Ch1 = 48V input, Ch2 = Iin, Ch3, VBUS and Ch4 IPMC output for all 4 plots

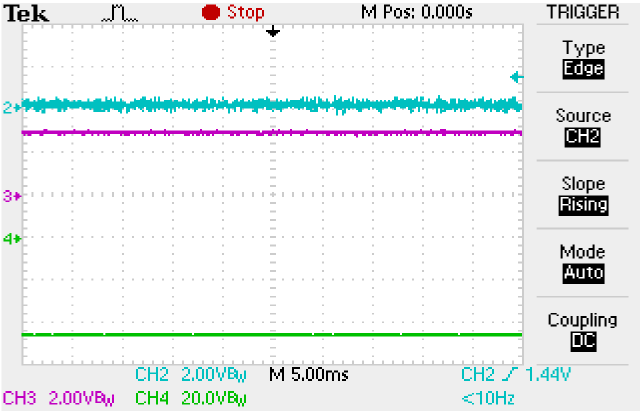
4.3. INPUT FET OR’ING FUNCTION

The module provides dedicated OR’ing of the –48V inputs and their corresponding returns. The IPSY200-XX-47 module replaces these diodes with FETs, which have intrinsic diode junctions and selectively switches the FETs on to reduce the volt drop across the diodes to near zero thereby increasing efficiency to in excess of 99%. This reduces the thermal problems associated with diode orring, increases the operating range of the DC DC converter whilst still maintaining the fundamental redundancy features necessary to maintain the supply under fault conditions. Plots 3-8 show the gate to source voltages of the channel FETS under different input conditions.



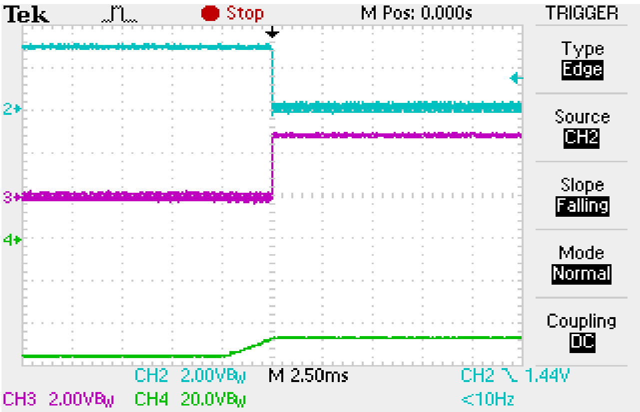
Ch2 Vgs VA FET
Ch3 Vgs VB FET
Ch4 VIN

Plot 5: Vgs VA , Vgs VB With 48Va input ON



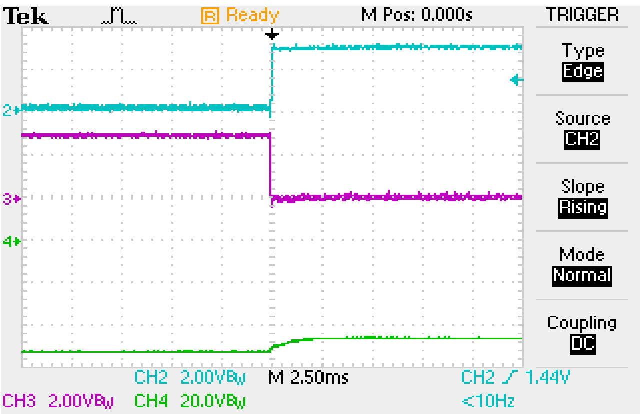
Ch2 Vgs VA FET
Ch3 Vgs VB FET
Ch4 VIN

Plot 6 Vgs VA , Vgs VB With 48Vb input ON



Ch2 Vgs VA FET
Ch3 Vgs VB FET
Ch4 VIN

Plot 7: Vgs VA , Vgs VB with input step change from 55V on 48Va to 48V on 48Vb.



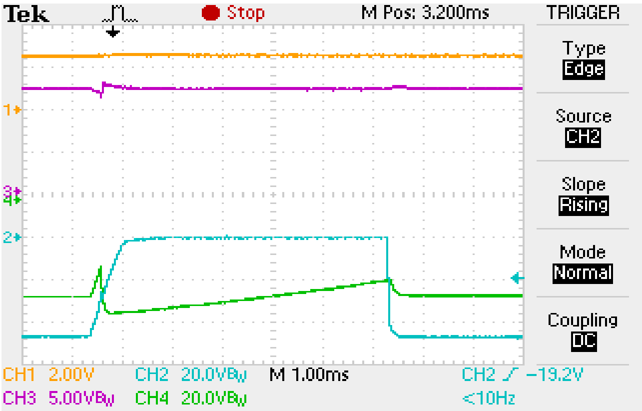
Ch2 Vgs VA FET
Ch3 Vgs VB FET
Ch4 VIN

Plot 8: Vgs VA , Vgs VB with input step change from 55V on 48Vb to 48V on 48Va

4.4. HOLD UP

The unique design feature of charging a bank of reservoir capacitors upto a regulated voltage of 59.5 volts provides a 5 X increase in energy storage capacity for a given volume of capacitance. The fact that this regulated voltage is within SELV limits means that no discharge resistor is required to ensure there are no hazardous voltages present on the module on turn off. Also another advantage of regulating the voltage to 59.5V volts is that 63V electrolytic capacitors can be used instead of the 100V capacitors that are normally required across the input supply. As the size of electrolytic capacitors is proportional to CV^2 this brings a dramatic reduction in the size of capacitors required to meet the hold up.

The reservoir capacitors take 30 seconds to charge up to the 59.5V volts to achieve the maximum hold up time of 8.4ms. The capacitors are held charged until the input supply falls below 40 volts. At this time all the input OR'ing MOSFETs are turned off and the output voltage is held up by the stored energy in the small capacitor across the input supply. After a short delay the reservoir capacitors are switched in parallel with the DC DC converter input to extend the running time of the converter by 8.4 milliseconds based on a 200W ATCA load. Plot 9 shows the hold up of the outputs when a short circuit has been placed on one of the –48V inputs.

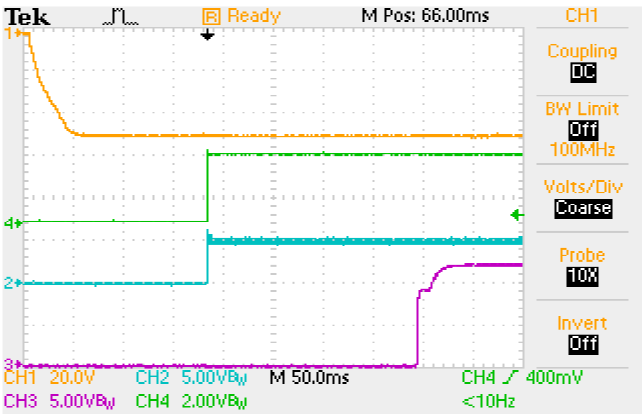


Ch1 3V3 IPCM
Ch2 VIN
Ch3 VBUS
Ch4 Boost switched in

Plot 9: Hold up of outputs under short circuit of input supply.

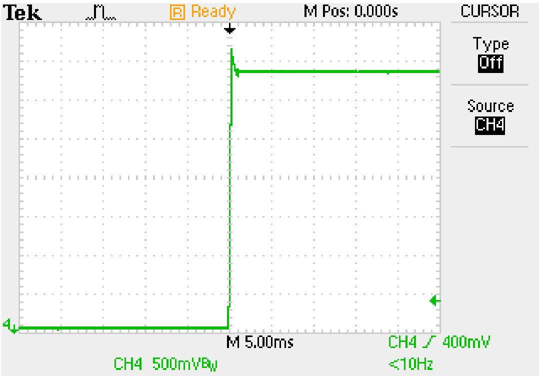
4.5. OUTPUT START UP WAVEFORMS

The waveforms in plots 10-14 show the start up waveforms of the 3V3IPMC and VBUS outputs at no and full load conditions. All of these waveforms have been taken with no extra load capacitance on the outputs.

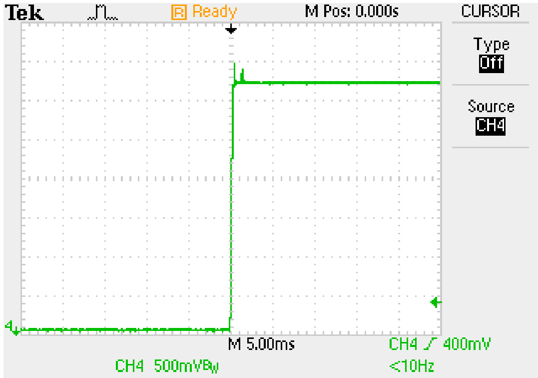


Ch1 48V input
Ch2 5VLED
Ch3 VBUS
Ch4 3V3IPMC

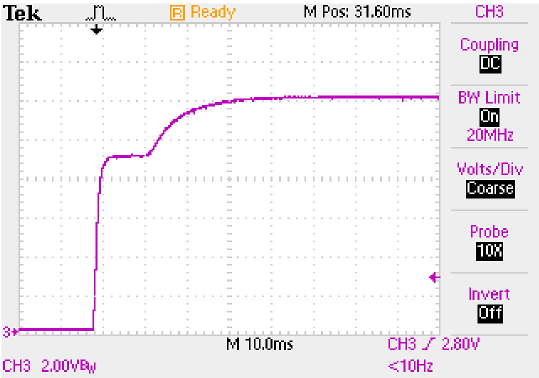
Plot 10: Output sequencing on application of enable signal. 48Va, 3v3IPMC, VBUS, 5VLED



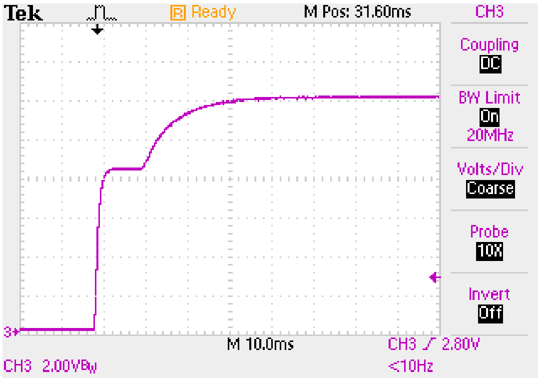
Plot 11: 3V3IPMC start up at no load



Plot 12: 3V3IPMC start up at full load



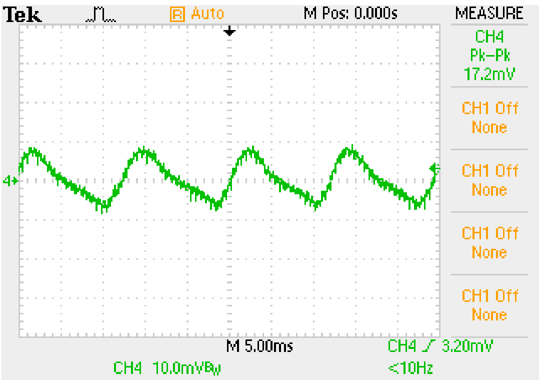
Plot 13: VBUS start up at no load



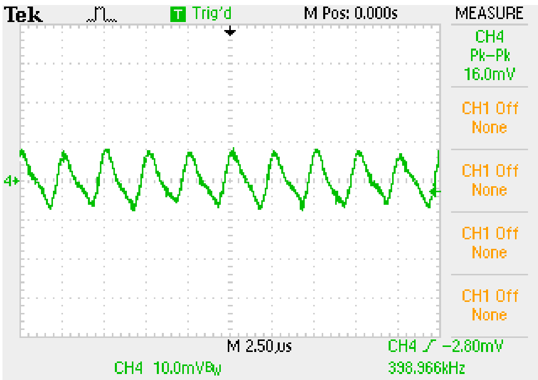
Plot 14: VBUS start up at full load

4.6. OUTPUT RIPPLE WAVEFORMS

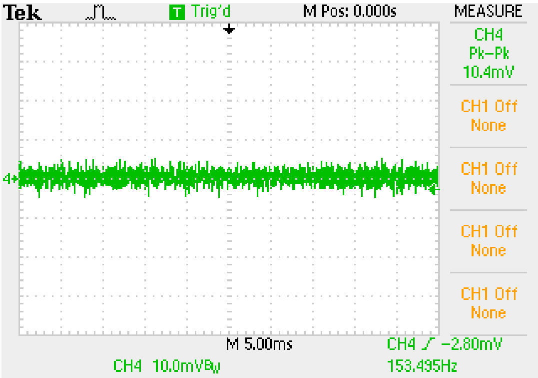
The waveforms in plots 15-18 show the output ripple voltage waveforms of the 3V3IPMC and VBUS outputs at no and full load conditions. All of these waveforms have been taken with no extra load capacitance on the outputs



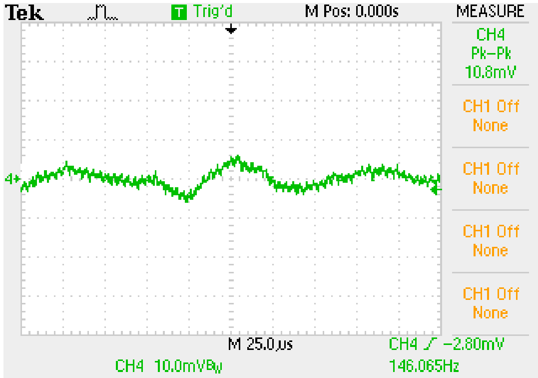
Plot 15: 3V3IPMC ripple LF



Plot 16: 3V3IPMC ripple HF



Plot 17: VBUS ripple LF



Plot 18: VBUS ripple HF

4.7. EFFICIENCY

The typical efficiency measurements of the IPSY200-XX-47 are as follows:

Vin	Iin	Pin	VBUS	VBUS LOAD	3V3 IPMC	3V3 IPMC LOAD	POUT	Overall Efficiency
40V	5.2A	208W	12.03V	14.4A	3.24V	2.00A	179.71	86.4%
48V	4.3A	206.4W	12.03V	14.4A	3.25V	2.00A	179.73	87.08%
60V	3.45A	207W	12.03V	14.4A	3.25V	2.00A	179.73	86.82%
72V	2.85A	205.2W	12.03V	14.4A	3.25V	2.00A	179.73	87.59%

Table 5: Efficiency measurements

4.8. MTBF CALCULATIONS

The calculated MTBF for the IPSY200-XX-47 is TBA hours as per MIL HDBK 217F

4.9. THERMAL PERFORMANCE

TBA

5. SOFTWARE

5.1. A TO D CONVERTER OPERATION

5.1.1. INTRODUCTION

The IPSY200-XX-47 module has a 6 differential channel Analogue to Digital converter incorporated into its design. This feature is incorporated so the IPSY200-XX-47 can provide a rough estimate of what input power is being taken through the dual redundant -48V inputs into each ATCA blade. The input power measurement is carried out by multiplying the lowest sampled signal of the voltage of the input supplies and a sample of the input current being drawn by the ATCA blade that has been sent to the local IPM Controller. 3 other channels are also digitally sampled so the IPM Controller can monitor the hot spot temperature of the particular blade ensure the blade is not dissipating excessive power plus each enable input is also monitored so the shelf manager can tell if any enable fuses have failed open circuit.

As all of the above signals are referred directly to the input supplies of the ATCA system and the IPM Controller is isolated and referred to the secondary side a method is required to transmit this data across the isolation barrier to the IPM Controller. This is achieved by using an I^2C bus and a standard isolation circuit. The next few sections will briefly describe what sampled signal is available on each of the 6 channels on the A/D, what there sampling rates per bit are on each channel and also what the address of the A/D is on the I2C bus so the IPM Controller can communicate with the A/D. The device that has been chosen to do this task is a MAX1028AEE from MAXIM. A more in depth description of the operation of this device can be found on the MAXIM datasheet.

5.1.2. ADDRESSING OF DEVICE ON I^2C BUS

The MAX1038 device used in the module is connected to an I^2C bus that is available on pins 7 and 10 of the 16 way SAMTEC connector of the IPSY200-XX-47 module. The device will normally sit in an idle state until a START condition is placed on the SDA line followed by the MAX1038 address. A START condition is a high to low transition on the SDA line with SCL high. The slave address for the MAX1038 has been factory programmed to 1100101X. The LSB of the address will be a 1 for reading data from the IC and a 0 for writing data to the IC. After receiving the address, the MAX1038 will issue an acknowledge by pulling SDA low for one cycle. The following block diagram explains the basic operation of the MAX1038:

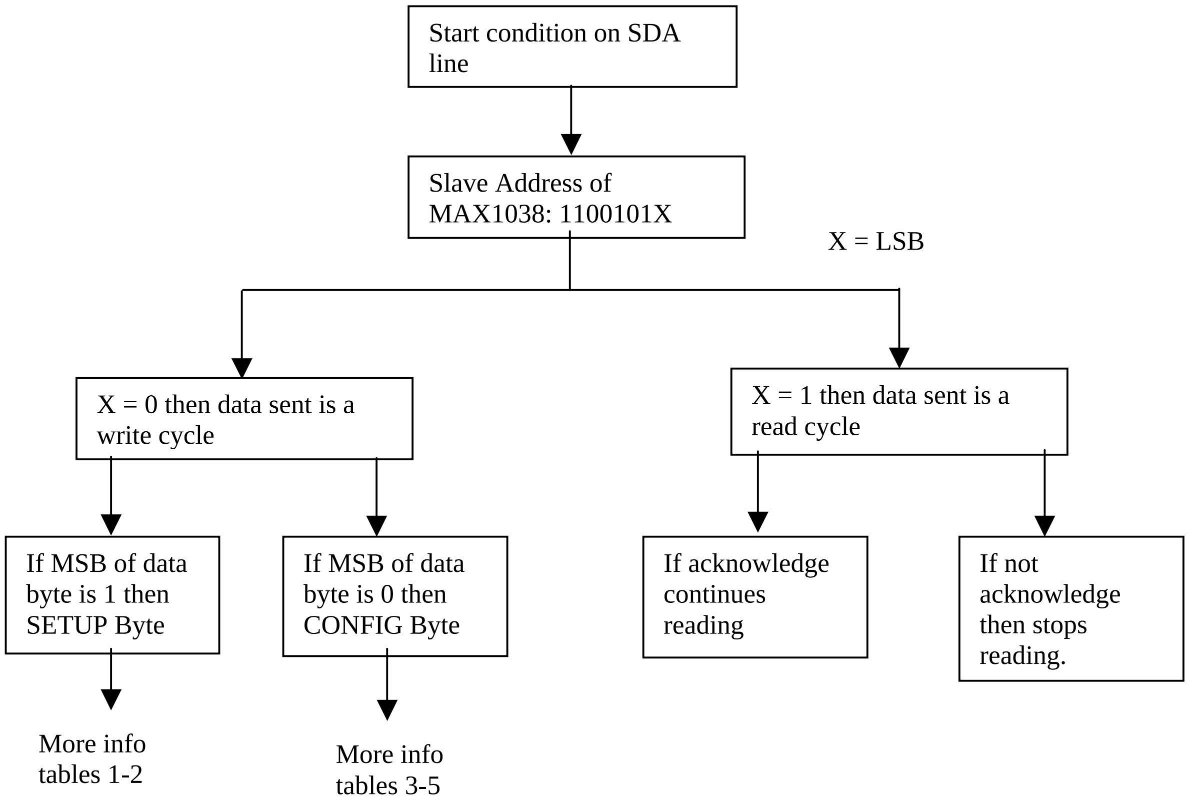


Figure 5: MAX1038 block diagram

5.1.3. CHANNEL IDENTIFICATION AND SCALING OF SIGNALS

5.1.3.1. SET-UP BYTE

There are two types of set up bytes on the MAX1038 device these are WRITE cycles and READ cycles. A WRITE cycle begins with a START condition being issued on SDA followed by the device slave address of 1100101 and a 0 on the LSB to signify a WRITE bit. If successful an acknowledge will be issued from the SLAVE (MAX1038) to the I^2C bus telling it to begin writing data. The SLAVE will recognise the next received byte as either a set up (see Table 6) or a configuration byte (see Table 8) by the value of the MSB. If the MSB is 1 then the byte is a set up byte and if the MSB is 0 then it is a configuration byte.

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
REG	SEL2	SEL1	SEL0	CLK	BIP/UNI	RST	X

BIT	NAME	DESCRIPTION
7	REG	Register bit. 1 = Set-up Byte, 0 =Configuration Byte (Table 8)
6	SEL2	Three bits select the reference voltage and the state of AIN_/REF (Table 7). **Default to 000 at power-up.**
5	SEL1	
4	SEL0	
3	CLK	1 = External Clock, 0 = Internal Clock. **Defaulted to 0 at power up.**
2	BIP/UNI	1 = Bipolar, 0 = Unipolar. **Defaulted to 0 at power-up**
1	RST	1 = No action, 0 = Resets the configuration register to default. Set-up register remains unchanged
0	X	Don't care, can be set to 1 or 0.

Table 6. MAX1038 Set-up Byte Format

The information in the table above describes the purpose of each bit in the set-up byte. Bit6 –Bit4 in the set-up byte selects the reference operation in the MAX1038 device. The information in table 7 shows all possible settings with regards to the reference. In all instances 101 should be the 3-bit code taken for this setting. This is because the internal reference is always used as the reference voltage due to the AIN11/REF input being an analogue input in the IPSY200-XX-47 circuit. The internal reference should always be ON as there are no spare pins on the device to connect to an external reference.
We recommend setting the CLK bit to a 0 to run of the internal oscillator in the device. The BIP/UNI bit should be set to UNIPOLAR (0) as all inputs to the MAX1038 are positive with respect to zero. The RST bit should normally be HIGH for no action.

This gives a recommended set-up byte of 1101001X for the IPSY200-12-47 module. This set-up byte has to be written to the MAX1038 via the I^2C before the A/D can be used for monitoring.

SEL2	SEL1	SEL0	REFERENCE VOLTAGE	AIN_/REF	INTERNAL REFERENCE STATE
0	0	X	V_{DD}	Analogue input	Always Off
0	1	X	External reference	Reference input	Always Off
1	0	0	Internal reference	Analogue input	Auto Shutdown
1	0	1	Internal reference	Analogue input	Always On
1	1	X	Internal reference	Reference input	Always On

Table 7. MAX1038 Reference Voltage and AIN_/REF Format

5.1.3.2. CONFIGURATION BYTE

As stated in section 5.1.3.1.of the application note if the MSB of the first data byte after a write condition is a 0 then the data byte is a configuration byte. Tables 8 –10 will describe in detail what the recommended configuration byte is for the IPSY200-XX-47 and also what other variations are possible if the end user prefers to use something different.

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
REG	SCAN2	SCAN0	CS3	CS2	CS1	CS0	SGL/DIF

BIT	NAME	DESCRIPTION
7	REG	Register bit. 1 = Set-up Byte, 0 =Configuration Byte
6	SCAN1	Scan select bits. Two bits select the scanning configuration (Table 9). **Default to 00 at power-up.**
5	SCAN0	
4	CS3	Channel select bits. Four bits select which analogue input channels are to be used for conversion (Table 10). **Default to 0000 at power-up.**
3	CS2	
2	CS1	
1	CS0	
0	SGL/DIF	1 = single-ended**, 0 = psuedo-differential** (Tables 10). **Default to 1 at power up**

Table 8. MAX1038 Configuration Byte Format

SCAN1	SCAN0	SCANNING CONFIGURATION
0	0	Scans up from ENBB to the input selected by CS3-CS0 (default setting)
0	1	Converts the input selected by CS3-CS0 eight times
1	0	Scans up from 48VA to the input selected by CS3-CS0. When CS3-CS0 is set for ENBB, ENBA or 48VB scanning stops at 48VB
1	1	Converts the channel selected by CS3-CS0

Table 9. MAX1038 Scanning configuration

The recommended configuration byte for the IPSY200-XX-47 is 00010100. This gives the end user the ability to read all 6 inputs simultaneously down the I^2C bus on the application of a read cycle after the slave address of the MAX1038. THE LSB OF THE CONFIGURATION BYTE SHOULD ALWAYS BE SET TO 0, AS SINGLE ENDED MEASUREMENTS WOULD BRING INVALID MEASUREMENTS.

Monitoring of individual channels on a read cycle is available by selecting the SCAN1 and SCAN 0 bits to 11 and by selecting the appropriate channel from table 10 below: For example the temperature of module is available by 01110000.

CS3	CS2	CS1	CS0	ENBB+ (AIN0)	ENBB- (AIN1)	ENBA+ (AIN2)	ENBA- (AIN3)	48VB+ (AIN4)	48VB- (AIN5)	48VA+ (AIN6)	48VA- (AIN7)	TEMP+ (AIN8)	TEMP- (AIN9)	48IN_I+ (AIN10)	48IN_I- (AIN11)
0	0	0	0												
0	0	1	0												
0	1	0	0												
0	1	1	0												
1	0	0	0												
1	0	1	0												

Table 10: IPSY200-12-47 A/D channel selection

The multiplying factor which should be used on these 6 channels for monitoring purposes are as follows:

Channel	Scaling Factor/bit
ENBB	0.5V
ENBA	0.5V
48VB	0.5V
48VA	0.5V
TEMP	0.090A
48IN_I	1.6°C

Table 11: A/D Scaling factors

Using the factors above means that the IPM Controller should be able to estimate the power consumption of each individual ATCA blade by using the 48VB or 48VA channel and 48IN_I channel.
Further information is available on the MAX1038 datasheet in terms of clocking speeds of I2C bus if required.

5.2. OUTPUT SEQUENCING OPERATION

5.2.1. INTRODUCTION

The IPSY200-XX-47 module also has the ability to monitor and sequence the start up of 3V3IPMC and 12V_VBUS. This task is achieved in the module by a SMS45 chip from SUMMIT electronics. The SMS45 is a non-volatile programmable voltage supply controller that can monitor and sequence 4 separate voltages during power up. Up to 4 output channels can be monitored continuously during start up and a logic level output OK signal is produced after a defined period of delay (t_{PDLY}) when the appropriate channel crosses its preset threshold. The output OK signal can then be used as part of the enable circuit of the next output to ensure that the correct sequencing occurs. See Figure 6 for the appropriate waveforms.

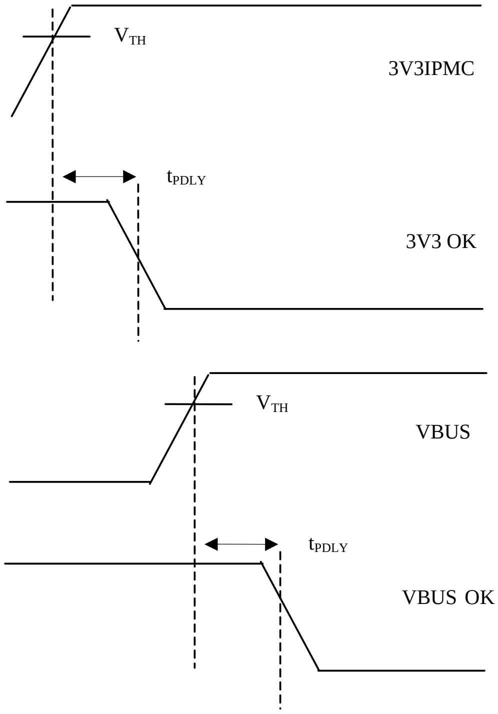


Figure 6: IPSY200-12-47 OUTPUT SEQUENCING

5.2.2. ADDRESSING OF DEVICE ON I²C BUS

The method of communication on the SMS45 chip is very similar to the MAX1038 described earlier. The SMS45 sits in an idle state until the SLAVE address of the SMS45 is seen following a START condition. The SLAVE address of the SMS45 is created as follows:

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB
Address Bits							
Device Type				Bus		MSB	R/W
SMS45				X	X	X	X
1	0	0	1	Configuration Register			
1	0	1	0	Memory(Default)			
1	0	1	1	Alternate Memory			

Table 12: SMS45 addresses

The internal memories available in the SMS45 are not used in the IPSY200-12-47 design so their operation will not be described in this application note. Their operation can be described in detail on the datasheet of the SMS45 from SUMMIT Microelectronics if using them is desirable.

The address bits for the bus (D3-D2) have been set by Visionpower to 00 and cannot be altered from this setting. With the MSB being a don't care and R/W being a 1 for READ and a 0 for WRITE this gives a device address of 100100X1 for READ operation to configuration registers and 100100X0 for WRITE operation to configuration registers. There are 8 configuration registers on the SMS45. These registers can be altered over the I2C bus to change the voltage levels that the output_OK signal will turn on at and also what time interval (t_{PDLY}) will take place between the start up. The 8 pre-programmed configuration registers of the SMS45 in IPSY200-XX-47 are shown in figure 7 below. This application note will describe in detail how these registers were obtained and also how these configuration registers can be altered to meet any variations that may be required in any other particular requirement.

NOTE: for performing a memory operation (Read or write) and to have the ability to change configuration register contents at least one supply input must be above 2.7V.

Checksum = AC (hex)

DESCRIPTION	Value	REG BITS
Trip Voltage 3	1.600	C03, D7-D0
Trip Voltage 2	2.295	C02, D7-D0
Trip Voltage 1	1.800	C01, D7-D0
Trip Voltage 0	3.000	C00, D7-D0
Reset Trigger Source V3	Asserts Reset Selected	C04, D7
Reset Trigger Source V2	Asserts Reset -Selected	C04, D6
Reset Trigger Source V1	Asserts Reset -Selected	C04, D5
Reset Trigger Source V0	Asserts Reset -Selected	C04, D4
Range Select V3	Low	C04, D3
Range Select V2	High	C04, D2
Range Select V1	High	C04, D1
Range Select V0	High	C04, D0
Sense Voltage V3-Over/Under	UV	C05, D3
Sense Voltage V2-Over/Under	UV	C05, D2
Sense Voltage V1-Over/Under	UV	C05, D1
Sense Voltage V0-Over/Under	UV	C05, D0
Reset Interval	200ms	C06, D6-D5
Longdog		C06, D4-D3
Watchdog	OFF	C06, D2-D0
Device Type Address	1010	C07, D6
2 to 3 Power Sequence Delay	50ms	C07, D5-D4
1 to 2 Power Sequence Delay	50ms	C07, D3-D2
0 to 1 Power Sequence Delay	50ms	C07, D1-D0

SMS45 Configuration Registers Programmed in IPSY200-XX-47

Register	Hexadecimal	Decimal	Binary
C0	50	080	01010000
C1	00	000	00000000
C2	21	033	00100001
C3	C8	200	11001000
C4	F7	247	11110111
C5	00	000	00000000
C6	62	098	01100010
C7	2A	042	00101010

Figure 7: SMS45 Configuration Registers

5.2.3. SUPPLY AND MONITOR FUNCTIONS

The V0, V1, V2, V3 inputs to the SMS45 are diode-OR'd so that any of the inputs can power the device supply. To achieve reliable operation one of the inputs must be greater than 2.7V. It is possible to sequence up to 4 outputs using the SMS45, in the IPSY200-XX-47 module the 3V3IPMC output and the 12V_VBUS are sequenced so that the 12V_VBUS cannot start up until the 3V3 reaches 3.00V provided the 3V3_OK signal is incorporated within the circuitry of the VBUS_ENABLE signal. The voltage to the input channel V1 has been scaled down so that a 2V input to SMS45 represents 12V on the output. It is possible to connect 2 further outputs to the SMS45 via the 16 way connector. These inputs to the SMS45 are available as follows:

Input Channel to SMS45	Output Voltage	Position on Connector
V0	3V3IPMC	
V1	12V_VBUS	
V2	EXTV1_MON	PIN 5 OF CON1
V3	EXTV2_MON	PIN 8 OF CON1

Table 13: SMS45 Output sequencing

The first four configuration registers of the SMS45 set the trip voltage level of each of the outputs. The thresholds can be programmed in small increments depending on what voltage range has been set for the output in configuration register 4, see section 5.2.4.If the range select is set to LOW then the voltage can be adjusted from 0.6V to 1.8V in 5mV increments and if it is set to HIGH it can be adjusted from 1.8V to 5.6V in 15mV increments.

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	ACTION
1	1	1	1	1	1	1	1	Highest threshold adjustment = 5.6V on HIGH range
0	0	0	0	0	0	0	0	Lowest threshold adjustment = 0.6V on LOW range
0	1	0	1	0	0	0	0	V0 register = 1.8V +(80*0.015V) = 3.00V
0	0	0	0	0	0	0	0	V1 register = 1.8V +(0*0.015V) = 1.80V
0	0	1	0	0	0	0	1	V2 register = 1.8V +(33*0.015V) = 2.295V
1	1	0	0	1	0	0	0	V3 register = 0.6V +(200*0.005V) = 1.60V

Table 14: SMS45 Configuration Registers 0-3

The 4 registers above can be altered to different levels if required provided the value of V0 is not greater than 3.3V and V1 is not greater than 2.0V on an undervoltage setting. If the thresholds were set above these levels then the OK_outputs signals will never change state

5.2.4. RESET AND U/V OR O/V FUNCTIONS

The reset function of the SMS45 can be activated by any combination of the four inputs V0-V3. The high-order 4 bits of configuration register 4 are used to specify what input channels will activate an output channel called RESET whenever an enabled under or overvoltage becomes active. The low-order 4 bits of configuration register 5 program the under and over voltage options of each channel. The RESET signal is available on pin 12 of the 16 way SAMTEC connector and is an open drain output. The RESET signal will stay LOW when the channel selected by register 4 exceeds its undervoltage level by a defined time period. The duration of the RESET is programmed by configuration register 6. The SMS45 has been programmed to give RESET lasting 200ms when any input rises above its undervoltage threshold stated in section 5.2.2 The low-order 4 bits on configuration register 4 are used to set the voltage range of the outputs

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB
V_3	V_2	V_1	V_0	V_3	V_2	V_1	V_0
RESET Trigger Source 1-Selected, 0- Off				Range Select 1-HIGH, 0-LOW			

Table 15: SMS45 Configuration Register 4

The status of the supplies fed into the SMS45 is available at any time over the I2C bus in the high order configuration bits of register 5(See table 16). A “1” in a bit location indicates a fault on that particular supply.

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB
V_3	V_2	V_1	V_0	V_3	V_2	V_1	V_0
FAULT CONDITION 1-FAULT, 0- OK				THRESHOLD SELECT 1-OVER, 0-UNDER VOLTAGE			

Table 16: SMS45 Configuration Register 5

5.2.5. CASCADING OF OUTPUTS AND TIMER SETTINGS

Configuration register 6 is used for setting the duration of the RESET and WATCHDOG timers and enabling the cascading of the outputs.

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	ACTION
CAS	**RTO1**	**RTO0**	**X**	**X**	**WD2**	**WD1**	**WD0**	
X	0	0	X	X	X	X	X	t_{PRTO} = 25ms
X	0	1	X	X	X	X	X	t_{PRTO} = 50ms
X	1	0	X	X	X	X	X	t_{PRTO} = 100ms
X	1	1	X	X	X	X	X	t_{PRTO} = 200ms
0	X	X	X	X	X	X	X	Cascade ON
1	X	X	X	X	X	X	X	Cascade OFF
X	X	X	X	X	0	0	0	WLDI = OFF
X	X	X	X	X	0	1	1	WLDI = 400ms
X	X	X	X	X	1	0	0	WLDI = 800ms
X	X	X	X	X	1	0	1	WLDI = 1600ms
X	X	X	X	X	1	1	0	WLDI = 3200ms
X	X	X	X	X	1	1	1	WLDI = 6400ms

Table 17: SMS45 Configuration Register 6

In the IPSY200-12-47 the WLDI timer is turned OFF, the reset timer(t_{PRTO}) is set to 200ms and the cascade off outputs is set to ON.

Configuration register 7 is used for setting the delay time (t_{PDLY}) between the input V0 going above the under voltage threshold and the output OK signal going low (See figure 4). The read/write protect bit of the configuration register 7 has been left enabled so the customer is able to alter any of the settings on the device. A = 1 and B = 0 has been chosen for the delays for PUP#1 to PUP#3.

D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	ACTION
		PUP#3		**PUP#2**		**PUP#1**		
CAS	**RTO1**	**Bit 1**	**Bit 0**	**Bit 1**	**Bit 0**	**Bit 1**	**Bit 0**	
X	0	A	B	A	B	A	B	DTI = 1010, responds only when Address bits = A2 & A1 logic states
X	1	A	B	A	B	A	B	DTI = 1011, responds only when Address bits = A2 & A1 logic states
0	X	A	B	A	B	A	B	Config. Reg, Read/Write enabled
1	X	A	B	A	B	A	B	Config. Reg. Read/Write locked out

Table 18: SMS45 Configuration Register 7

A	B	t_{PDLY}
0	0	0ms Delay
0	1	25ms Delay
1	0	50ms Delay
1	1	100ms Delay

Table 19: SMS45 Configuration Register 7

There is a 4k-Bit nonvolatile memory available for use in the SMS45 device on the IPSY200-12-47 but as it is not proposed to be used by VISIONPOWER there is no detailed explanations of its operation. If this is an added feature that would be of interest then further information is available on the SMS45 datasheets.